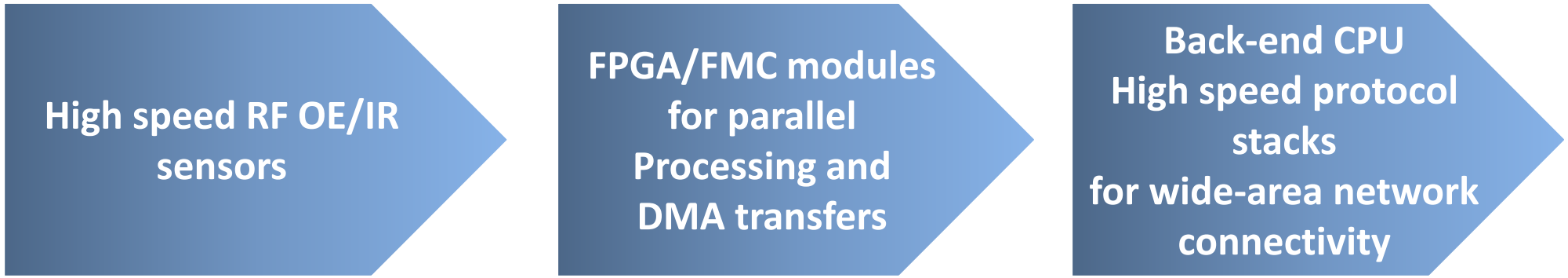
INTERFACE CONCEPT
ADVANCED ELECTRONIC SOLUTIONS
www.interfaceconcept.com

High speed data communication in HPEC VPX 6U platforms



Sensors including RF Sampling or high Resolution cameras

Low Power Parallel Processing on sample data Very high-speed Transceivers

High-end processors Wide-band on the backplane Multi-Root Complex Communication

Why high speed data communication is of the essence?

- HPEC systems are used in performing SWaP constrained UAVs, UGVs and UUVs programs
- HPEC systems combine FPGA modules and DSP boards tightly coupled together.
- Signal acquisition interface with new JSED204B high speed ADCs using the GTX/GTH/GTY transceiver technology of Xilinx (up to 30 Gb/s on the GTY transceivers of Ultra Scale FPGAs)
- Fast FPGA processing on samples : FPGAs feature a very good ratio parallel processing power to consumption (10 times better than a processor for algorithms like FFT)
- Move huge quantity of processed sampling data from FPGA memory to processor memory for further processing with a minimum latency
- High speed communication required between SWaP constrained SIGINT, Radar, EW, Search and Track systems

OpenVPX standard is the best available standard on the market allowing HPEC high speed data transmission.

Control and Data Plane strategy

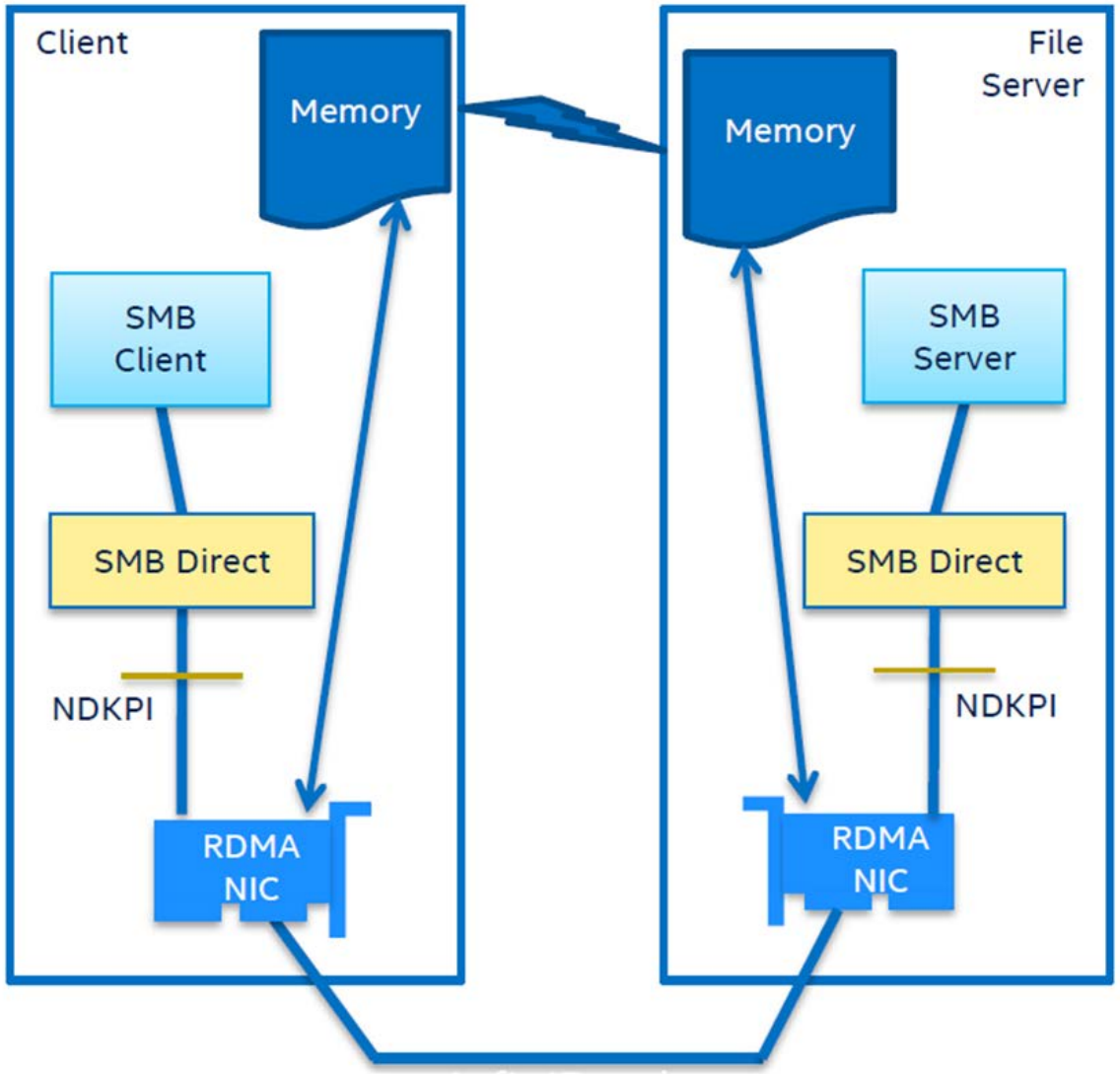
- Data Plane:
  - PCIe switch fabric combined with Multiware
    - Non-transparent bridging (Multi-RC)
    - Status report (linked, speed, width)
    - NT windows size & prefetch mode configuration
    - Multicast and Dual cast
    - Independent Management port
    - H Topology
    - RDMA API (beta Q3/2016)
  - 10/40G Ethernet Data Plane under development :
    - low latency Cut-through architecture
    - High-performance dual engine with a throughput up to 640Gb/s
    - Low Power engine with a throughput up to 240Gb/s
    - RDMA convergence
- Control Plane: Giga Ethernet Switch (a real standard today)

OpenVPX™

Cometh 4410a

RDMA Convergence

- Accelerated IO delivery model which works by allowing application software to bypass most layers of software and communicate directly with the hardware
- Benefits:
  - Low latency
  - High throughput
  - Zero copy capability
  - OS/Stack bypass



New Multiware Software layout

For PCIe seamless communication between Root Complex